Memory Organizations for 3D Die Stacking

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Abstract

This talk provides a brief overview of die-stacking technologies, covering some of the different options out there for stacking. I will then focus on architectural approaches for 3D-stacked memories, as this is one of the first major application areas of die stacking. For markets that require significant memory capacity and upgradable memory, die-stacked DRAM alone will not be sufficient, which creates technical challenges for the architecture and overall system organization. This talk will focus on techniques to integrate the stacked memory in a software-transparent fashion, but we will also discuss challenges and open research directions for exposing the heterogeneity of this kind of memory system to the software stack.

Bio

Gabriel H. Loh is a Fellow Design Engineer in AMD Research, the research and advanced development lab for Advanced Micro Devices, Inc. Gabe received his Ph.D. and M.S. in computer science from Yale University, respectively, and his B.Eng. in electrical engineering from the Cooper Union. Gabe was also a tenured associate professor in the College of Computing at the Georgia Institute of Technology, a visiting researcher at Microsoft Research, and a senior researcher at Intel Corporation. He is a senior member of IEEE and distinguished scientist of the ACM, (co-)inventor on over eighty US patent applications and twenty-seven granted patents, and a recipient of the U.S. National Science Foundation Young Faculty CAREER Award. His interests include computer architecture, processor microarchitecture, memory systems, emerging technologies, 3D die stacking, cooking and eating, ice hockey, and endurance sports.