Virtual Memory for Next-Generation Multi-Tier Memory Architectures

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Abstract

Virtual memory offers a simple hardware abstraction to programmers freeing them from the tedious process of manual memory management. However, the emergence of new memory technologies are posing problems for conventional virtual memory. Homogeneous memory systems are being replaced by complex heterogeneous systems with multiple memory devices with different latency, bandwidth, and capacity characteristics. These heterogeneous memory systems require frequent data movement to take advantage of these different memory devices.

This work upgrades virtual memory to effectively support heterogeneous memory systems. The goal is to provide high-performance data management and scalable address translation coverage. To achieve the goal, this dissertation shows that modest hardware and software changes are sufficient. It proposes three techniques – a lightweight hardware address translation coherence approach; a high-throughput software page migration infrastructure; and OS support to defragment memory such that it becomes easier to generate large swaths of translation contiguity that can be covered with few TLB entries. In total, contribution of this dissertation is to identify bottlenecks in the existing virtual memory systems, to profile the performance impacts of these bottlenecks, and to provide hardware and software solutions in the context of heterogeneous memory systems.

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